SUB-MICRON SILICON RF IC TECHNOLOGIES: "An Overview"

David K. Lovelace, Jesus L. Finol and Jeffrey C. Durec
Motorola Semiconductor Products Sector
2100 East Elliot Rd. (MD:EL379)
Tempe, Arizona 85284-1801, USA

Abstract- **Silicon based semiconductors have become the standard active device technology of choice in today's cost and performance driven consumer wireless products. No longer is silicon technology confined to low frequency analog and digital processing functions. Silicon devices have now reached high frequency performance levels which allow them to be used almost exclusively in the RF section of many wireless communication circuits. This paper will deal with the issues involved in employing silicon IC technologies to low cost, low power, RF circuits.**

I. ACTIVE DEVICE CHARACTERISTICS

Wireless applications require IC processes that are specifically optimized for high frequency analog circuits. The performance characteristics for active devices used in low voltage wireless applications can generally be quantified by the following important parameters:

- Cut-off frequency (f_τ)
- Maximum frequency of oscillation (f_{MAX})
- Noise figure (NF)
- Flicker noise (1/f noise)
- Saturation voltage
- Early Voltage (V_A) in bipolar junction transistor (BJT) devices and channel length modulation (λ) in MOSFET devices

A. Device Frequency Characteristics

Schematics of the simplified small-signal models used to define f_τ and f_{MAX} for the BJT and the MOSFET are shown in Fig. 1. These models have been abbreviated so as to reduce the complexity of the equations defining f_τ and f_{MAX}. f_τ is defined as the frequency at which the common emitter or common source short-circuit current gain becomes unity. This parameter allows the designer to gauge the frequency capabilities of a device. A common "rule of thumb" is to use a device with an f_τ at least ten times greater than the intended frequency of operation. For example, in a 900MHz application, a transistor with an f_τ of at least 9GHz would be required.

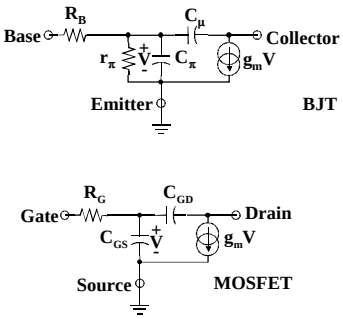

Fig. 1. Simplified BJT small-signal model used to calculate the device f_τ and f_{MAX}.

The equation defining the f_τ of a BJT is given by (1) and that of a MOSFET is given by (2).

$$f_{\tau[BJT]} = \frac{g_{m[BJT]}}{2\pi(C_\pi + C_\mu)} \quad (1)$$

$$f_{\tau[MOSFET]} = \frac{g_{m[MOSFET]}}{2\pi(C_{GS} + C_{GD})} \quad (2)$$

The transconductance terms of both the BJT and MOSFET are defined to first order by Equations (3)[1] and (4)[2] respectively.

$$g_{m[BJT]} = \frac{qI_C}{kT} \quad (3)$$

$$g_{m[MOSFET]} = \mu C_{OX}\frac{W}{L}(V_{GS} - V_t) \quad (4)$$

Note that unlike the BJT equation for transconductance (3), the MOSFET transconductance (4) does not explicitly show its dependence on temperature variations. Both the mobility and the threshold voltages of the MOSFET are affected by temperature and its dependence on temperature is shown in (5) and (6)[3] [1].

$$\mu = K_\mu T^{-1.5} \quad (5)$$

$$V_t(T) = V_t(T_0) - \alpha(T - T_0) \quad (6)$$

It can be seen from (3) and (4) that the transconductance of a BJT is dependent on temperature and collector current and that of the MOSFET is dependent not only on the bias condition V_{GS}, but also on device size parameters defined by the ratio of the gate width to the gate length of the device and to the process dependent parameters μ, C_{OX} and V_t.

Finally, the f_τ of a device is strongly dependent on bias and device size or area. The device area relates directly to the size of the capacitance terms, and in the case of the MOSFET, to the transconductance as well. It is important to remember these points because many manufacturers quote f_τ for a minimum geometry device operated at very high current density. This is often misleading since a minimum geometry device is often not an optimum size used for many RF applications. RF transistors are usually larger devices and are not operated at their maximum current density.

f_{MAX} is defined as the frequency when the unilateral power gain (7)[4] becomes unity [2]. Equation (7) assumes that the imaginary component of the input and output admittances are removed through matching. When this condition is met, the effects of the parasitic collector-substrate capacitance (C_{CS}) and the drain-source capacitance (C_{DS}) are not taken into account. Perhaps an alternative to the f_{MAX} figure of merit would be the frequency at which the open circuit voltage gain becomes unity.

The equations defining f_{MAX} for both the BJT (8) and the MOSFET (9) look almost identical to each other.

$$G_U = \frac{|y_{21}|^2}{4\mathrm{Re}(y_{11})\mathrm{Re}(y_{22})} \quad (7)$$

$$f_{MAX[BJT]} = \sqrt{\frac{f_{\tau[BJT]}}{8\pi R_B C_\mu}} \quad (8)$$

1. q is the charge of an electron, k is Boltzman's constant, T is temperature (°K) and I_C is the collector current
2. μ is the surface mobility of the channel, C_{OX} is the capacitance per unit area of the gate oxide, W is the effective channel width, L is the effective channel length, V_{GS} is the voltage applied to between the gate and source nodes and V_t is the threshold voltage.
3. K_μ and α are process dependent constants
4. y_{21} is the device forward transconductance, y_{11} is the device input admittance and y_{22} is the device output admittance

0-7803-4471-5/98/$10.00 (c) 1998 IEEE

$$f_{MAX[MOSFET]} = \sqrt{\frac{f_{\tau[MOSFET]}}{8\pi R_G C_{GD}}} \quad (9)$$

f_{MAX} is more representative of the resulting RF performance of a device than f_τ since it takes into account the series base or gate resistance which play a major role in the frequency and noise performance of a device. A good RF device should have an $f_{MAX} > f_\tau$, and the best RF devices have an $f_{MAX} > 2f_\tau$.

B. Noise Characteristics

Noise in an active device generally falls into two regions, the flicker noise or 1/f noise contribution and the thermal noise contribution. The flicker noise contribution occurs at low frequencies and the frequency in which the flicker noise falls to the level of the thermal noise, is called the 1/f corner frequency (f_c). Fig. 2 shows the relationship of these two noise contributions versus frequency [3].

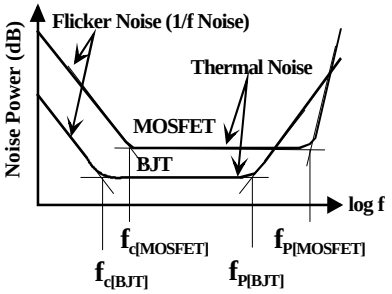

Fig. 2. Contributions of both Flicker Noise (1/f Noise) and Thermal Noise vs. Frequency

The noise figure of an RF device is an important parameter that quantifies the signal-to-noise ratio degradation which is caused by a device. Noise figure is restricted to the thermal noise contribution in the context of this paper. Noise figures of the BJT and the MOSFET [3] for $f > f_c$ are shown in (10)[1] and (11) respectively[2]:

$$NF(f)_{[BJT]} = 10\log\left[1 + \frac{1}{R_S}\left(R_B + \frac{1}{g_{m[BJT]}}\right) + \frac{R_S g_{m[BJT]}}{2|\beta(jf)|}\right] \quad (10)$$

$$NF(f)_{[MOSFET]} = 10\log\left[1 + \frac{1}{R_S}\left(R_G + \frac{2}{3g_m}\right) + \frac{2R_S(2\pi f C_{GS})^2}{3g_m}\right] \quad (11)$$

Note the frequency dependence of the noise figure. The frequencies in which the noise figure increases is defined by the roll off in the transistor gain and is given by (12) for the BJT and by (13) for the MOSFET.

$$f_{P[BJT]} = \frac{f_{\tau[BJT]}}{R_B g_{m[BJT]}} \quad (12)$$

$$f_{P[MOSFET]} = \frac{f_{\tau[MOSFET]}}{R_G g_{m[MOSFET]}} \quad (13)$$

The definition of the minimum source impedance[3] is given by [3]. Using (10) and (11) the optimum source impedance can be determined for each device[4] given by (14) for the BJT [3] and by (15)[5] for the MOSFET.

$$R(f)_{Sopt[BJT]} = \frac{\sqrt{|\beta(jf)|}}{g_{m[BJT]}}\sqrt{2R_B g_{m[BJT]} + 1} \quad (14)$$

$$R(f)_{Sopt[MOSFET]} = \frac{1}{2\pi f C_{GS}} \quad (15)$$

From these equations it is evident that the BJT requires a lower source impedance than that of the MOSFET in order to achieve a minimum noise figure at frequencies less than f_P. This is an important fact that shows the limits on the usefulness of MOSFETs for RF circuits. In most RF circuit environments a source impedance of 50Ω is typically used which is difficult to transform into a high impedance required to minimize the noise figure of the MOSFET.

The minimum noise figure can be calculated by substituting the optimum source impedance back into the noise figure equations. Substituting (14) into (10) yields the minimum noise figure for the BJT given by (16) [3] and substituting (15) into (11) yields the minimum noise figure for the MOSFET.

$$NF(f)_{opt[BJT]} = 10\log\left[1 + \frac{1}{\sqrt{|\beta(jf)|}}\sqrt{2R_B g_m + 1}\right] \quad (16)$$

$$NF(f)_{opt[MOSFET]} = 10\log\left[1 + 2\pi f C_{GS}\left(R_G + \frac{4}{3g_{m[MOSFET]}}\right)\right] \quad (17)$$

Flicker noise is a low frequency noise contribution that impacts the performance of audio frequency circuits and direct conversion receivers, but it also contributes noise at high frequencies due to frequency translation and perturbation of RF oscillators. Noise sources modulate RF oscillators producing unwanted sideband noise referred to as phase noise. Typically, flicker noise is the dominant noise source in oscillator circuits [4]. The oscillator phase noise gets mixed with the incoming wanted RF signal, and results in unwanted noise at the translated frequency.

MOSFETs have a 1/f corner frequency about ten times higher than that of BJTs [5]. This often results in unacceptable oscillator noise performance, necessitating the use of BJTs for RF oscillators. The phase noise of an oscillator and its dependence on f_c is given by (18)[6] [7].

$$L(f_m) = 10\log\left\{\left[1 + \frac{f_o^2}{(2f_m Q_{load})^2}\right]\left(1 + \frac{f_c}{f_m}\right)\frac{FkT}{2P_{sav}} + \frac{2kTRK_o^2}{f_m^2}\right\} \quad (18)$$

C. DC Operating Constraints

An important parameter to consider in low power RF circuit design is the supply voltage in which the circuit operates. Because of device breakdown parameters, a high voltage limit of operation is established, but this limit is very seldom encountered in today's wireless applications. Often a very low power supply voltage is applied to the RF circuitry. This presents a design problem since it limits the number of active devices that can be "stacked" between the supply voltage. For example, to operate within a 1V power supply, only one V_{BE} (~0.7V) and a $V_{CE(SAT)}$ (~0.2V) can be stacked between the power supply. Because the base-emitter and saturation voltage characteristics of a BJT are consistent, it is a better choice for use in low voltage RF circuits. A BJT exhibits an exponential collector current versus base-emitter voltage characteristic over a range of about nine

1. $\beta(jf) = \dfrac{\beta_{DC}}{1 + j\left(\dfrac{f}{f_\tau}\right)\beta_{DC}}$
2. R_S is the impedance of the driving source
3. The impedance of the driving source
4. $R_{Sopt} = \sqrt{\dfrac{\overline{v_i^2}}{\overline{i_i^2}}}$
5. Assuming that $R_G \ll \dfrac{8kT}{3g_{m[MOSFET]}}$
6. $L(f_m)$ is the ratio of sideband power in a 1Hz bandwidth at f_m to total power in dB, f_m is the frequency offset from the carrier, f_o is the carrier frequency, f_c is the flicker noise corner frequency, Q_{load} is the loaded Q of the tuned circuit, F is the noise factor (*Noise Figure* = 10log[F]), k is Boltzman's constant, T is temperature (°K), P_{sav} is the average power of the oscillator input, R is the equivalent noise resistance of the tank circuit and K_o is the oscillator voltage gain.

decades. The MOSFET should not be operated in the weak inversion or the velocity saturation region thus limiting its useful drain current range to about two decades [5]. This concept can be illustrated by Fig. 3 which shows that the MOSFET has a much lower transconductance than the BJT for the same amount of current.

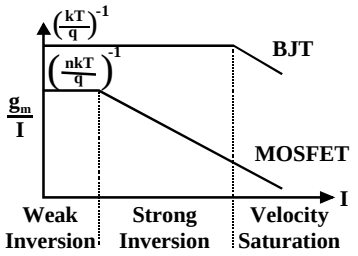

Fig. 3. g_m/I versus collector and drain current for a BJT and MOSFET [5]

Neglecting the effects of series extrinsic resistance, the saturation voltage of the BJT is within a few kT/q and is defined by (19)[1] [6] and the MOSFET saturation voltage is set by its W/L ratio and is defined by (20) [5]. In order for the MOSFET to achieve low saturation voltages, the size of the device gate length must increase, thus limiting the high frequency performance of the device due to increased capacitance. This saturation voltage limitation coupled with high threshold voltages limit the usefulness of MOSFETs in low voltage high performance RF applications. The effects of various gate W/L ratios on MOSFET saturation voltages are shown in Fig. 4 which also shows a typical value for a BJT saturation voltage for comparison.

$$V_{CEsat} = \frac{kT}{q}\ln\left(\frac{1+\beta_R}{\beta_R}\right) \tag{19}$$

$$V_{DSsat} = \sqrt{\frac{2I_D}{\mu C_{ox}\frac{W}{L}}} \tag{20}$$

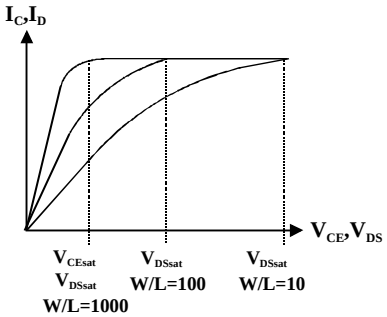

Fig. 4. Comparison of MOSFET and BJT saturation voltages [5]

The output impedance of a high frequency BJTs and MOSFETs is lower than that of low frequency devices. This limits the usefulness of high frequency devices in DC bias applications. The BJT Early voltage (V_A) and the MOSFET channel length modulation parameter can be related to the small signal output resistance (r_o) by the following equations[2]:

$$r_{o[BJT]} = \frac{V_A}{I_C} \tag{21}$$

$$r_{o[MOSFET]} = \frac{1}{\lambda I_D} \tag{22}$$

A more complete model of the device output impedance would include the parasitic capacitance elements, thus making the output impedance frequency dependent. Equations (23)[3] and (24)[4] define the output impedance of the BJT and MOSFET and the expressions are plotted in Fig. 5.

$$Z(f)_{o[BJT]} = \frac{r_{o[BJT]}}{j2\pi f r_{o[BJT]}[C_{CS}+C_\mu]+1} \tag{23}$$

$$Z(f)_{o[MOSFET]} = \frac{r_{o[MOSFET]}}{j2\pi f r_{o[MOSFET]}[C_{DB}+C_{GD}]+1} \tag{24}$$

Due to the design constraints in creation of a device with high f_τ and f_{MAX}, the output resistance parameter suffers. A MOSFET can regain some output resistance by making the device gate length longer (decreasing λ as shown in (25)[5] [5]) at the expense of high frequency performance, unlike a BJT where the Early voltage is a function of the base width and is an established process parameter. As in the MOSFET case, increasing the BJT output resistance is done at the expense of high frequency performance. Note that for the BJT, $f_\tau \propto \tau_f^{-1}$ and that by increasing the effective base width (W_B), τ_f increases, causing f_τ to decrease (26)[6] [3], but V_A increases (27) [3].

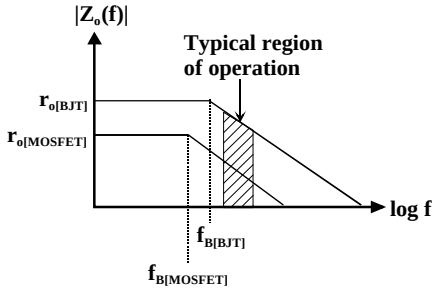

Fig. 5. Frequency dependence of device output impedance.

$$\lambda = \frac{1}{V_E L} \tag{25}$$

$$\tau_f = \frac{W_B^2}{2D_n} \tag{26}$$

$$V_A = W_B\frac{dV_{CE}}{dW_B} \tag{27}$$

II. SIGNAL ISOLATION

Signal isolation is paramount to good silicon IC RF design. If signals (at any frequency) are allowed to interact with each other, performance is degraded.

Consider for example a 900MHz receiver with a $1V_P$, 100MHz digital signal (assuming a square wave) occurring on the same IC. A first order determination of what the IC isolation requirements must be so that the 9th harmonic of the digital signal does not de-sensitize the receiver is given below: Assume that the receiver must have a sensitivity of at least -115dBm[7] (~$400nV_{RMS}$). The

1. β_R is the reverse DC current gain
2. V_A is the BJT Early voltage, I_C is the BJT collector current, λ is the MOSFET channel length modulation parameter and I_D is the MOSFET drain current
3. C_{CS} is the BJT collector-substrate capacitance
4. C_{DB} is the MOSFET drain-bulk capacitance
5. V_E is the MOSFET Early voltage per unit-channel length, analogous to the BJT Early voltage V_A.
6. D_n is the diffusion constant for electrons

0-7803-4471-5/98/$10.00 (c) 1998 IEEE

ninth harmonic of the 100MHz digital signal falls within the receive band at a power level of -19dBm[1] (~25mV$_{RMS}$). Therefore at least 96dB of isolation is required to reduce the interference level of the digital signal to the minimum sensitivity of the receiver. This simplistic example shows how important isolation is to silicon wireless IC design.

Fig. 6 shows a diagram of an RF signal isolation test structure. Note the use of low resistance substrate contacts to form isolation rings. This test structure is used to evaluate and model the performance of RF isolation techniques used on an IC. Results from measurements of the RF isolation structure is shown in Fig. 7. Note that all measurements were made with a vector network signal analyzer with contacts to the substrate made from the top side of the die, as would a real application of an IC, not with an unrealizable bottom substrate ground contact. Connections to the substrate are important. The substrate must be well grounded since it is a collector of the parasitic signals from the active and passive devices located directly above it.

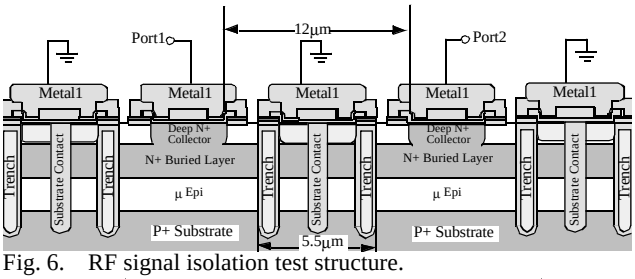

Fig. 6. RF signal isolation test structure.

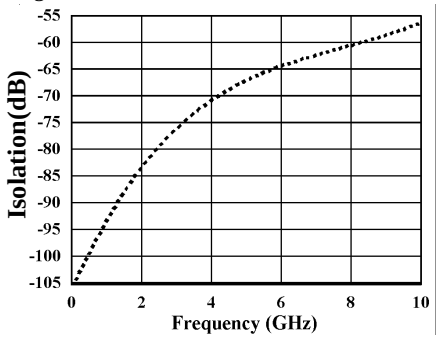

Fig. 7. Measured port to port isolation of the test structure shown in Fig. 6

III. SUMMARY

An overview of the technological aspects to achieve high levels of RF and IF integration has been presented. Many of the important active device characteristics required for a silicon IC process used for high frequency wireless applications have been shown. Based on this information, the BJT is still the device of choice for low power, high performance RF applications, and MOSFETs for power amplifiers and high density digital applications. It is a system requirement to segregate the high frequency functions because of the isolation levels required. Combining mixed signal circuits onto a single IC should only be done at frequencies low enough so that the die and package isolation permit their integration. A block diagram showing the best use of available silicon IC technology paired to a generic transceiver is shown in Fig. 8. IC solutions for wireless applications will only become more viable when they are not only cheaper than discrete devices, but they must also perform as well as or exceed the performance of discrete devices.

7. Assuming power referenced to 50Ω

1. Assuming power referenced to 50Ω

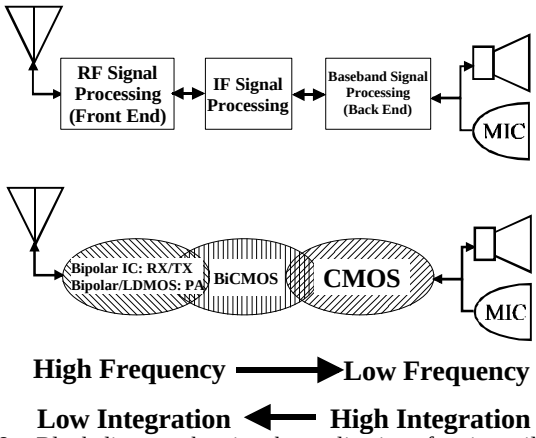

Fig. 8. Block diagram showing the application of various silicon technologies to a generic transceiver.

The goal of many research and development activities being conducted in industries and universities is to reduce cost and improve performance of wireless communication products and services. It seems clear that to achieve higher levels of RF/IF integration, basic architectural changes are needed to realize single chip solutions; allowing CMOS a more active participation. A possible scenario could be to integrate those functions where CMOS does not penalize the system from a power dissipation point of view and leave the high-frequency blocks to more current drain efficient technology such as BJT and BiCMOS technologies. This, however, leads us to the conclusion that single chip solutions for portable wireless transceiver, based on present data, is not a viable solution as the literature is suggesting. CMOS devices with comparable performance to bipolar counterparts are needed. But, scaling techniques used to improve CMOS performance, are applicable to bipolar transistors as well. Although single chip solutions have been shown to be "functional" [12-13], there has yet to be a single-chip solution with performance approaching the performance of state of the art multi-chip, multiprocess system solutions.

References

[1] P.E. Allen, D.R. Holberg. *CMOS Analog Circuit Design*, Fort Worth: Holt, Rinehart and Winston, Inc., 1987.

[2] G.A.M. Hurkx, "The Relevance of f_τ and f_{MAX} for the Speed of a Bipolar CE Amplifier Stage," *Proceedings of the IEEE BCTM*, pp. 53-56, Sep. 1996.

[3] P.R. Gray, R.G. Meyer. *Analysis and Design of Analog Integrated Circuits: Third Edition*, New York: John Wiley and Sons, Inc., 1993.

[4] U.L. Rohde. *Microwave and Wireless Synthesizers: Theory and Design*, New York: John Wiley and Sons, Inc., ch. B, 1997.

[5] K.R. Laker, W.M.C. Sansen. *Design of Analog Integrated Circuits and Systems*, New York: McGraw-Hill, Inc., ch. 2, 1994.

[6] I. Getreu. *Modeling the Bipolar Transistor*, Beaverton: Tektronix, Inc., 1976.

[7] U.L. Rohde, T.T.N. Bucher. *Communications Receivers: Principles and Design*, New York: McGraw-Hill, Inc., ch. 7, pg. 302, 1988.

[8] L. E. Larson. *RF and Microwave Circuit Design for Wireless* Communications. Boston: Artech House.

[9] I.A. Koullias, et. al., "A 900MHz Transceiver Chip Set for Dual-Mode Cellular Radio Terminals," *Proc. Int. Solid-State Circuits Conf.*, San Francisco, CA, pp. 140-141, 1993.

[10] T. Stetzler, et. al., "A 2.7V to 4.5V Single-Chip GSM Transceiver RF Integrated Circuit," *Proc. Int. Solid-State Circuits Conf.*, San Francisco, CA, pp. 150-151, 1995.

0-7803-4471-5/98/$10.00 (c) 1998 IEEE